Amendments to the Specification:

Please amend the title as follows:

METHOD AND SYSTEM TO VERIFY A CIRCUIT DESIGN BY VERIFYING CONSISTENCY BETWEEN TWO DIFFERENT LANGUAGE REPRESENTATIONS OF A CIRCUIT DESIGN.

Please replace paragraph [0016] with the following amended paragraph:

[0016] In block 106, an unwinding bound may be entered by a user for a second computer language representation of the device or circuit design. The unwinding bound may also be entered into a command line or by an interactive input. The second computer language representation may be a program language, such as a C-type language or ~~the like~~ other type programming language. In contrast to the unwinding bound for a HDL or Verilog® representation of a device, there may be multiple inputs or bounds for a programming language because there may be multiple loops in a program language or C-type program representation of a device or circuit design. Entering an unwinding bound for the second computer representation or program language representation may be optional in at least one embodiment in that the method 100 may be adapted to automatically increase an unwinding depth if necessary.

Please replace paragraph [0018] with the following amended paragraph:

[0018] In block 112, a correspondence between the two bit vector equations may be checked or determined by conjoining the equations and passing them to a decision procedure 114 that may use a SAT procedure or ~~the like~~ a similar decision procedure. The decision procedure 114 will return a satisfyability result in block 116. An example of a decision procedure that may use a SAT procedure or the like in accordance with an embodiment of the present invention will be described in more detail with respect to

Figure 5. The decision procedure 114 may return whether the conjoined equation is satisfiable or not. That is, whether there exists an assignment to the variables within the equation that makes the equation "true." If the equation is not satisfiable in block 118, the method 100 may advance to block 120 and no violation of any claim was found in the decision procedure 114. Thus, no mismatch exists between the first or HDL representation of the device and the second or program language representation of the device within the unwinding depth entered by the user. The method 100 may output a "Programs are Consistent" message or indication that may be displayed or presented on an output device of a system such as system 600 to be described with reference to Figure 6. The method may then end at termination 122.